SEMICONDUCTOR PACKAGE

CROSS REFERENCE TO RELATED APPLICATION

This application is based on and claims priority to United States Provisional Patent Application No. 60/101,810, filed September 25, 1998, entitled SEMICONDUCTOR PACKAGE, the entire disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention is related to a semiconductor package in which a semiconductor die is disposed between upper and lower plate members and, more particularly, to an SO8 semiconductor package in which a source of a MOSFET semiconductor die is electrically coupled to a leadframe via an upper plate member while the MOSFET gate is electrically coupled to the leadframe via a wire bond.

2. Related Art

With reference to Fig. 1, a semiconductor package 10 according to the prior art is shown. The semiconductor package 10 includes a bottom plate portion 13 and terminals 12a, 12b. A semiconductor die 16 is disposed on top of the bottom plate portion 13 and fastened thereto, typically using an epoxy material. The semiconductor die 16 includes a metalized region 18 (typically aluminum) defining a connection area for a top surface of the semiconductor die 16. Portions of the

terminals 12a, 12b, bottom plate portion 13, and semiconductor die 16 are encapsulated in a housing 22, typically formed from a moldable material. In order to obtain an electrical connection between the metalized region 18 and the terminal(s) 12b, one or more wires 20 are ultrasonically bonded at one end 21a to the metalized region 18 and at a distal end 21b to the terminal 12b.

Fig. 2 shows another semiconductor package 100 of the prior art. In order to electrically connect the metalized region 18 with the terminal 12b, one or more wires 24 are stitch bonded at locations 23, thereby providing additional paths for current to flow from the semiconductor die 16 to the terminal 12b. This marginally reduces the resistance of the current path from the semiconductor die 16 to the terminal 12b.

It is desirable to significantly reduce the resistance and inductance of current paths through a power semiconductor package in order to ensure optimum performance of the semiconductor device. Unfortunately, the semiconductor packages of the prior art do not fully achieve this objective because, among other things, the distance D between one area of the metalized region 18 and the end 21a of the wires 20 increases the resistance of the current path from the metalized region 18 to the terminal 12b. This problem is exacerbated when the thickness of the metalized region 18 is relatively small (typically, the thickness is approximately 4 to 8 microns). The relatively thin metalized region 18 in combination with the distance D and the cross sectional profile of the wire bond 20 results in a relatively high resistance and inductance for the current path therethrough.

In some packages (for example S08 packages) the distance D is approximately 80 to 100 mils resulting in a resistance of between about 0.79 and 1.58 mohms for the metalized region 18. The diameters of the wires 20, 24 are approximately 2 mils yielding resistances of about 1.05 mohms (when 14 wires are used). With terminal and epoxy resistances aggregating to about 0.307 mohms, such packages exhibit total resistances of between about 2.14 to 2.93 mohms. The resulting package thermal resistance, RJA, can reach 62.5 °C/W.

When the semiconductor package 10 includes, for example, a MOSFET semiconductor die 16, the resistance caused by the distance D and the relatively small diameter of the wires 20, 24 adds to the overall resistance of the MOSFET. Indeed, when die 16 is a MOSFET die, the terminals 12a are typically coupled to the drain of the MOSFET while the terminals 12b are coupled to the source of the MOSFET via one or more wire bonds 20. As ON resistances of MOSFET dies become smaller and smaller, the resistance caused by the distance D and the wire bonds 20, 24 become a larger and larger portion of the overall resistance from one terminal 12a to another terminal 12b. Of course, the high frequency performance of a semiconductor device, like a MOSFET, is significantly effected by the resistance and inductance from terminal to terminal through the device.

Some prior art packages have incorporated a large metal strap to obtain an electrical connection between the metalized region 18 and terminal 12b. Unfortunately, this technique has only been possible in large semiconductor packages having relatively simple surface structures, such as bipolar junction transistors,

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diodes, and thyristors. Further, the metal straps were not practical in small outline packages (such as S08, surface mount dual in line packages).

The use of a large metal strap in a MOS-gated device, such as a MOSFET, has not heretofore been achieved because such devices have relatively complex surface structures. In particular, MOS-gated devices typically include a gate runner (or bus), disposed on the surface of the semiconductor die, which traverses the surface such that gate potential is distributed over the surface of the die. Consequently, disposing a large metal strap over the surface of the die has been problematic because the gate runner restricts access to the die surface and could be shorted to the metal strap. Thus, the use of metal straps in MOS-gated semiconductor devices has been prohibitive.

Accordingly, there is a need in the art for a new semiconductor package which overcomes the deficiencies in the prior art semiconductor packages by, among other things, reducing the resistances of the current paths through MOS-gated devices and reducing the inductances of such current paths.

SUMMARY OF THE INVENTION

In order to overcome the deficiencies of the prior art, a semiconductor package according to one aspect of the instant invention includes a bottom leadframe having a bottom plate portion and at least one first terminal extending from the bottom plate portion; at least one second terminal being co-planar with the first terminal; a semiconductor power MOSFET die having a bottom surface defining a drain connection and a top surface on which a first metalized region defining a

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source and a second metalized region defining a gate are disposed, the bottom surface being coupled to the bottom plate of the leadframe such that the first terminal is electrically connected to the drain; a copper plate coupled to and spanning a substantial part of the first metalized region defining the source connection; and at least one beam portion being sized and shaped to couple the copper plate portion to the at least one second terminal such that it is electrically coupled to the source.

BRIEF DESCRIPTION OF THE DRAWINGS

For the purpose of illustrating the invention, there are shown in the drawing forms which are presently preferred, it being understood, however, that the invention is not limited to the precise arrangements and instrumentalities shown.

Fig. 1 is a side view of a semiconductor package according to the prior art;

Fig. 2 is a side view of a semiconductor package according to the prior art;

Fig. 3 is a side view of a semiconductor package according to the present invention;

a1 a2

Fig. 4 is a top plan view of a1 the semiconductor package shown in Fig. 3;

a2 Fig. 5 is a top plan view of an alternative embodiment of the semiconductor package of Fig. 4;

Fig. 6 is a sectional view of the semiconductor package of Fig. 5 taken along line 6-6;

Fig. 7 is a cut-away perspective view of an alternative embodiment of the semiconductor package of the instant invention;

Fig. 8 is a cut-away perspective view of another alternative embodiment of the semiconductor package according to the instant invention; and

Fig. 9 is a cut-away perspective view of still another alternative embodiment of the semiconductor package according to the instant invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawing wherein like numerals indicate like elements, there is shown in Fig. 3 a perspective view of a semiconductor package 110 in accordance with one aspect of the present invention. The semiconductor package 110 includes a semiconductor die 16 having a bottom surface coupled to a bottom plate 13. Preferably, the semiconductor die 16 is a MOSFET die and terminals 12a are electrically coupled to the drain of the MOSFET die 16. Of course, the semiconductor die 16 may take on other forms, such as diodes, insulated gate bipolar transistors, or the like.

The semiconductor die 16 includes a top surface having a metalized region 18 which defines a connection to the semiconductor die 16. For example, when the semiconductor die 16 is a MOSFET, metalized region 18 may define a source connection.

The semiconductor package 110 also includes a strap member 28 which is employed to electrically couple the metalized region 18 to the terminals 12b. Each strap member 28 preferably includes a substantially thick plate portion 30 and a shaped beam portion 34. The plate portion 30 is preferably formed of copper and spans a substantial portion of the metalized region 18. The beam portion 34 is shaped and sized to couple the plate portion 30 to the terminals 12b.

Preferably, the beam portion 34 is coupled, at one end, to a lateral edge of the plate portion 30 and includes a distal end 36 which is coupled to a respective terminal 12b.

A curable conductive material 46 (such as silver filled conductive epoxy) is preferably disposed between the lower surface of the plate portion 30 and the metalized region 18 such that the plate 30 is firmly coupled to the metalized region 18. Soft solder may also be used. DLC. 11/18/98 CCH 12/18/98

It is preferred that the semiconductor package 110 include a housing 22 formed from a moldable material (such as plastic) and that the package configuration conforms to the SO8 standard.

Advantageously, the strap member 28 provides a relatively large contact area for coupling the terminal 12b to the metalized region 18, thereby reducing resistance to current flow and reducing inductance. This provides for improved performance at high frequencies. Further, this structure also enjoys the advantage of providing a thermal path for heat to escape the semiconductor die 16 through the strap member 28.

As best seen in Figs. 4 and 5, which show top plan views of the semiconductor package 110, the beam portion 34 is preferably integrally formed into one flowing member which extends from one lateral edge of the plate portion 30 and terminates at the terminals 12b.

a3 a3

A metalized region 19 defines a gate of the MOSFET die 16. The metalized region 19 is electrically coupled to one terminal 12b via wire bond 20. Thus, the present invention employs a mixed connection to the MOSFET die 16 top surface, namely, a low resistance plate portion 30 for connecting to the source and a wire bond 20 for connecting to the gate 19.

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As best seen in Fig. 5, a gate runner (or bus) 19a couples the gate metalized region 19 to the source areas of the surface of the die 16. It is preferred that the plate portion 30 extend laterally beyond outermost portions of the gate runner 19a. It is also preferable that the plate portion 30 extend beyond and cover as much of the gate runner 19a as possible. This ensures that improved performance is achieved.

Fig. 6 shows a sectional view taken along line 6-6 of Fig. 5. A portion of the gate runner 19a is shown disposed between metalized region 18. Preferably, a solderable metal (such as TiNiAg) is disposed on top of the metalized region 18. In order to insulate the gate runner 19a from the plate portion 30, a nitride layer 27 is disposed on top of the gate runner 19a. The curable conductive material 46 (preferably silver filled epoxy) is disposed on top of the solderable metal 25 and electrically and mechanically couples the plate portion 30 to metalized regions 18. Advantageously, the plate portion 30 is electrically and thermally coupled to the metalized regions 18 without interfering with the gate runner 19a.

It is noted that the plate portion 30 may be soldered to the solderable metal 25 if desired. It is preferred, however, that the silver filled epoxy 46 be employed to couple the plate portion 30 to the metalized region 18. When conductive epoxy 46 is employed, it is noted that the solderable metal 25 may be eliminated and the epoxy may directly contact the metalized region 18.

Reference is now made to Fig. 7 which shows an alternative embodiment of the present invention. In particular, the distal end of the beam portion 34 includes a heel 37 and toe 38 which creates a void 42

proximate to the terminal 12b. Preferably, the distal end of the beam portion 34 includes a downwardly directed projection 40 which extends through the void 42 toward the terminal 12b. It is preferred that curable conductive material 44 is introduced into the void 42 to facilitate electrically and mechanically coupling the distal end of the beam portion 34 to the terminal 12b. A suitable curable conductive medium 44 for use with the present invention may be selected from any of the known conductive epoxies or the like (silver filled epoxy being preferred).

Reference is now made to Fig. 9 which shows a cut-away perspective view of a semiconductor package 116 according to another aspect of the present invention. The semiconductor package 116 of Fig. 8 is substantially the same as the packages of the previous embodiments except that the plurality of beam portions 34 terminate at a cross bar portion 50. The cross bar portion 50 is coupled to at least two terminals 12b.

Preferably, the cross bar portion 50 includes a longitudinal heel 52 and a longitudinal toe 54 defining a void located proximate to the terminals 12b. The void 56 is in the form of a channel extending for substantially the entire length of the cross bar portion 50. It is preferred that the cross bar portion 50 include a downwardly directed projection 58 (in the form of a wall) extending through the channel toward the terminals 12b. A layer of curable conductive material (such as conductive epoxy) is preferably disposed within the channel to couple the cross bar portion 50 to the terminals 12b.

Reference is now made to Fig. 8 which show a cut-away perspective view of a semiconductor package 118

according to another embodiment of the present invention. The semiconductor package 118 is similar to the previous embodiments of the present invention except that the plate portion 30, beam portions 34 and terminals 12b are all integrally coupled and preferably formed from a common sheet of material. Thus, terminal 12b extends from outside the housing 22 into an interior of the housing and substantially over the top portion of the semiconductor die 16 to sandwich the semiconductor die 16 between the top and bottom plate portions 30 and 13, respectively.

It is noted that the metalized regions 18 may be formed from a solderable metal (such as copper, gold, silver, or the like) and that a plurality of flowable conductive bumps (preferably solder bumps, not shown) may be disposed on the surface of the metalized regions 18. Further, the plate portion 30 may include a lower surface which is oriented in an opposing fashion to the flowable conductive bumps such that the plate portion 30 may electrically and/or mechanically engage the flowable conductive bumps and the metalized regions 18.

The lower surface of the plate portion 30 may also include one or more downwardly directed projections extending from the plate portion 30 towards the flowable conductive bumps and the metalized regions 18.

It has been found that when that plate portion 30 is about 0.108 x 0.104 mils, the resistance introduced into the package is only about 0.115 mohms. Using metalized regions 18 aggregating about 0.08 mohms, the total package resistance according to the invention is only about 0.506 mohms (a 50% to 75% improvement over the prior art packages). Further, the thermal resistance RJA

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of the package of the instant invention is only about 46 °C/W max (a 25% reduction over the prior art packages).

The foregoing description of the preferred embodiments of the present invention have been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention be limited not be this detailed description, but rather by the claims appended hereto.